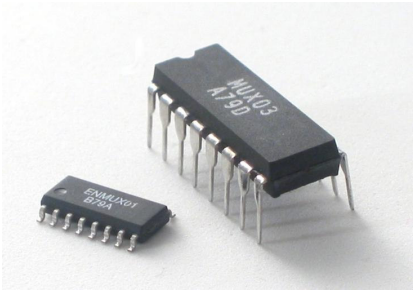
Multiplexer for Capacitive Sensors (MUXC01)



Features

- Very well suited for multiple-capacitance measurement
- Low-cost CMOS
- Low output impedance
- Rail-to-rail digital outputs
- All inputs and outputs are ESD protected
- High digital output currents possible (8 mA at 10% voltage drop)
- Large capacitive driving capability
- Available in 16-pins DIL(MUX03) in 16-pins SOIC(MUXEN01) and as bare die(MUXC01)
- Temperature range -40ºC to 85ºC

1. General Description

The multiplexer chip (MUXC01) is designed to select the passage-path of the digital signals between one input and nine outputs. It is mainly composed of a basic 9-bit shift register (nine cascaded D-flipflops) and nine 2-input AND gates (see Figure 2).

The square-wave signal is entered through the signal input (*signal in*) of the MUXC01. The input signal is gated by the nine 2-input AND gates to the respective 9 outputs (*OUT1 ~ OUT9*). One of two inputs of the AND gates is controlled by the output Q_i of the D-flipflops. If the input signal of the MUXC01 keeps high (V_{CC}), the function of the MUXC01 just is a 9-bit shift register with one data entry (*serial in*) and the output from each of the nine stages. The *shift out* is internally connected to the data output of the shift register via an output buffer. The shift output can be used as an input for a second MUXC01, for instance, when more than nine capacitances are to be measured.

The outputs of the MUXC01 are:

$$OUT_i = SignalIn \cdot Q_i \quad (i = 1, 2, \cdots 9) \tag{1}$$

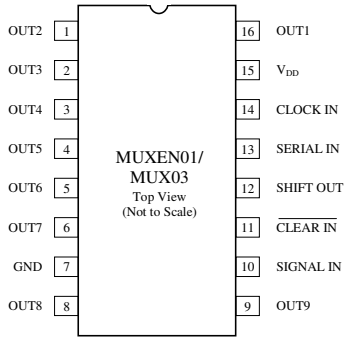
$$ShiftOut = Q_9 \tag{2}$$

where *SignalIn* is the input signal at the *signal in* terminal and *ShiftOut* is the output signal at the *shift out* terminal.

The states of the 9-bit shift register are determined by the three control inputs: the *serial in*, the *clock in* and the $\overline{clear\ in}$ The serial input is used as data entry to create an arbitrarily bit pattern at the outputs of the MUXC01. Each low-to-high transition on the clock input shifts data one place to the right and enters into Q_1, the serial input, the data that existed before the rising clock edge. A low level on the $\overline{clear\ in}$ overrides all other inputs and clears the nine outputs (*OUT1 ~ OUT9*) and shift output asynchronously, forcing all outputs low level. Figure 3 shows the timing diagram of the MUXC01.

2. Pin-out and Ratings

The MUXC01 is available in a 16-pin plastic dual-in-line package (DIP) as well as a 16-lead small outline package (SOIC). Figure 1 shows the pin configuration of DIP and SOIC. The function of the pins is listed in Table 1.



16-pins DIL(MUX03) and SOIC(MUXEN01)

Figure 1 Pin configuration.

Pin No.	SYMBOL	Function of the pin
15	V_{DD}	Positive supply voltage
16, 1, 2, 3, 4, 5, 6, 8, 9	OUT1 ⋯ OUT9	Outputs
10	SIGNAL IN	Signal input
11	$\overline{CLEAR\ IN}$	Master reset input (Active Low)
12	SHIFT OUT	Shift output
13	SERIAL IN	Data input
14	CLOCK IN	Clock input (Low to High edge triggered)
7	GND	Ground (0 V)

Table 1. Function of the pins.

3. Truth Table

Table 2 Truth table of the MUXC01.

INPUTS				OUTPUTS			
$\overline{CLEAR\ IN}$	*CLOCK*	*SERIAL IN*	*SIGNAL IN*	*OUT1*	*OUT2*	……	*OUT9*
L	×*	×	×	L	L	……	L
H	↓	×	×	NO CHANGE			
H	↑	L	×	L	*OUT1n* *	……	*OUT8n*
H	↑	H	×	H	*OUT1n*	……	*OUT8n*

* Note: 1. ×: Don't care,
2. *OUT1n* ~ *OUT8n*: The output of *OUT1* ~ *OUT8*, respectively, before the most-recent positive transition of the clock.

4. Logic Diagram

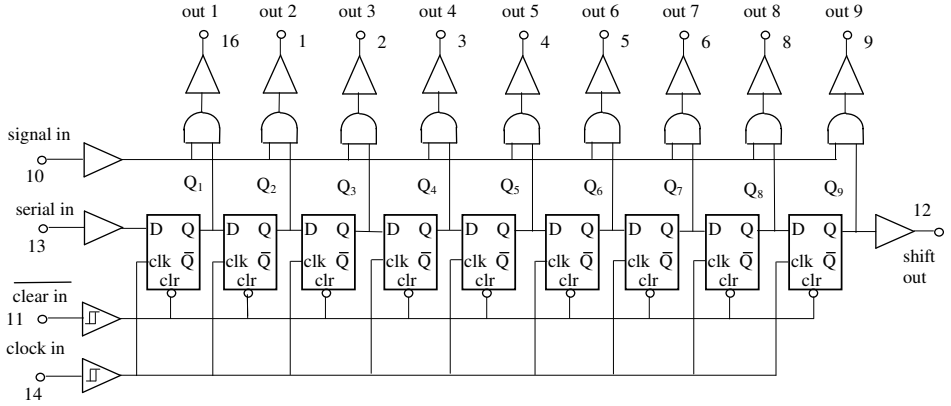


Figure 2 The internal diagram of the MUXC01.

5. Timing Chart

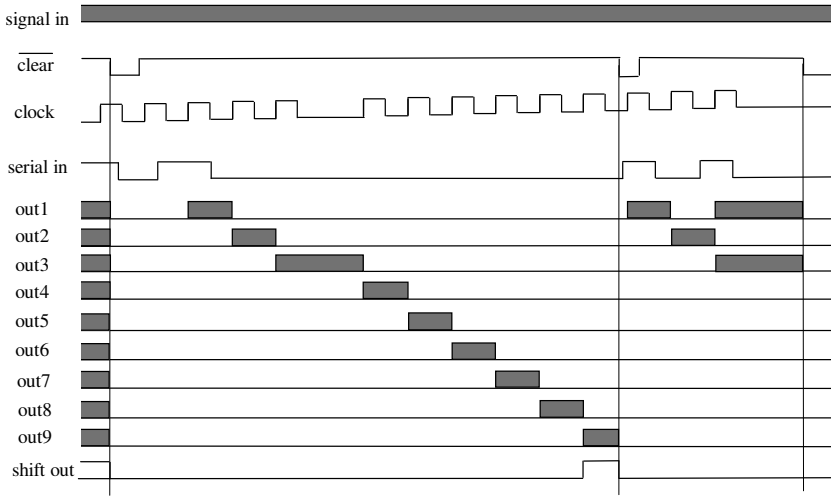


Figure 3 The timing diagram of the MUXC01.

6. Input and Output Equivalent Circuit

The MUXC01 has been fabricated in a low-cost 0.7-µm CMOS technology. The output buffers have a drive capability of 8 mA. A CMOS schmitt trigger input buffer has been used as the input stage of the *clear in* and *clock in* to eliminate the effect of the interference at these inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage. Figure 4 shows the input and output equivalent circuit.

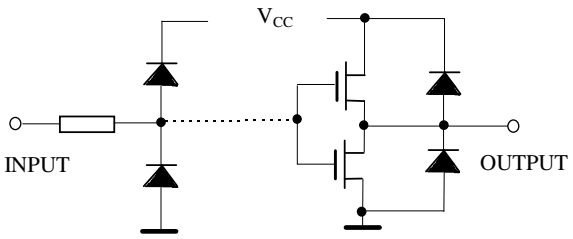


Figure 4 The input and output equivalent circuit.

7. Absolute Maximum Ratings

T_A = +25 ℃	
Power supply voltage	-0.3 V to +7 V
Power dissipation	500 mW
DC input voltage	-0.3 V to V_{DD}+0.3 V
Output current	8 mA
Output impedance	60 Ω
DC output voltage	-0.3 V to V_{DD}+0.3 V
DC Input current on each pin	±20 mA
ESD rating	> 4000 V
Storage temperature range	-65°C to +150°C
Operating temperature range	-40°C to +85°C
Lead temperature (soldering, 10 sec)	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation under these conditions is not implied.

8. DC Specifications

Table 3 shows some DC parameters of the MUXC01 under the conditions of V_{CC} = 5 V±10%.

Table 3 Some DC parameters.

Symbol	Parameters	min.	typ.	max.	Unit
I_0	Output current			8	mA
V_{CC}	Supply voltage	2.7	5	6	V
ΔV_{out}	Output voltage deviation between any 2 of 9 output (in same package)		0.1		mV
R_0	Output resistance		13		Ω
ΔR_0	Output resistance deviation between any 2 of 9 output (in same package)		0.6		Ω
V_{IH}	High level input voltage	3.5			V
V_{IL}	Low level input voltage			1.5	V
V_{OH}	High level output voltage	4.0			V
V_{OL}	Low level output voltage			0.25	V
I_{CC}	Quiescent supply current		0.38		µA

9. AC Electrical Characteristics

Table 4 shows some AC parameters of the MUXC01 under the conditions of V_{CC} = 5 V ± 10%, frequency of the input signal of 100 kHz and no external load.

Table 4 Some AC parameters.

Symbol	Parameters	min.	typ.	max.	Unit
$t_W(L)$	Minimum Pulse Width ($\overline{\text{CLEAR}}$)	–	10	20	ns
$t_W(L)$, $t_W(H)$	Minimum Pulse Width (CLOCK)	–	10	20	ns
$t_W(L)$, $t_W(H)$	Minimum Pulse Width (SIGNAL IN)	–	8	15	ns
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$ -OUT)	–	23	36	ns
t_{PHL}, t_{PLH}	Propagation Delay Time (CLOCK-OUT)	–	23	36	ns
t_{PLH} t_{PHL}	Intrinsic propagation delay time (Signal In-OUT_i)		9.8 10.5		ns
t_{TLH} t_{THL}	Output transition time		13.9 12.9		ns
f_{MAX}	Maximum clock frequency	30	50		MHz
C_{load}	Output capacitive drive capability			15	nF
B	HF bandwidth for signal input		1.6		MHz
C_{IN}	Input capacitance		5	10	pF
C_{PD}*	Power Dissipation Capacitance		111		pF

* Note C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current is: $I_{CC(opr)} = C_{PD}V_{CC}f_{IN}+I_{CC}$. Figure 5 shows the testing circuit for current $I_{CC}(Opr)$.

Figure 6 and Figure 7 show the output resistance R_0 vs the power supply voltage V_{CC} and the load current for V_{CC} = 5V±10%, respectively.

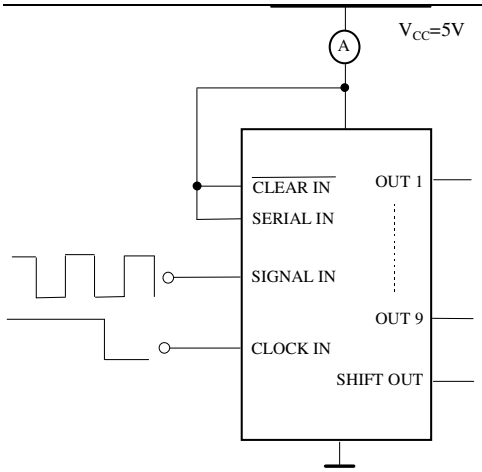


Figure 5 The testing circuit for $I_{CC(opr)}$.

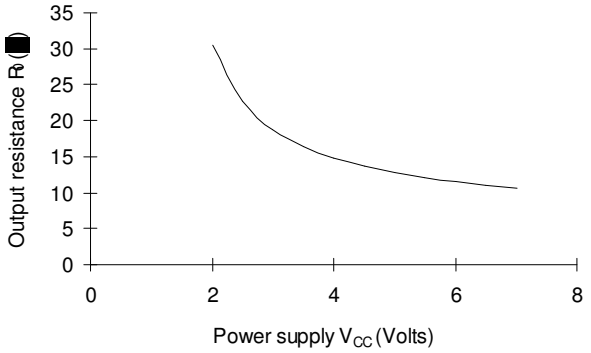


Figure 6 Output resistance vs power supply voltage.

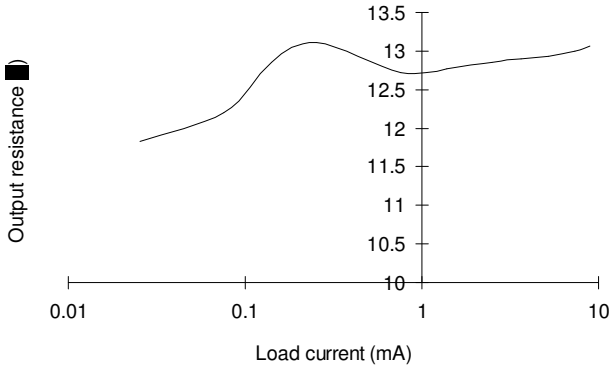


Figure 7 Output resistance vs the load current.

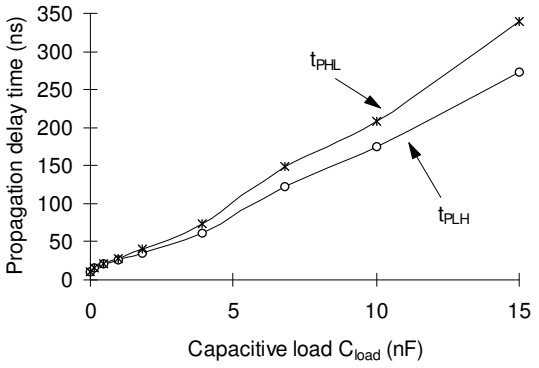


Figure 8 The propagation delay times of the multiplexer.

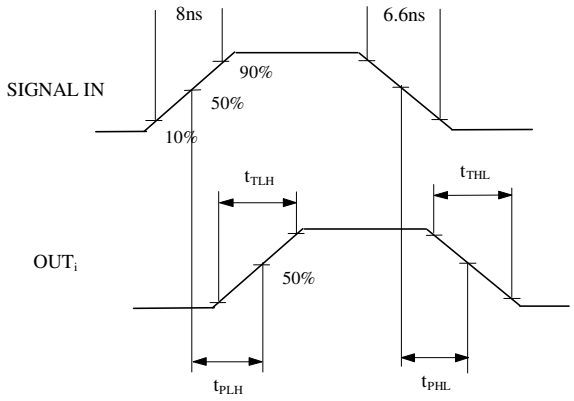


Figure 9 The AC characteristics test waveforms.

10. Applications

A. Multiple capacitance measurement

The MUXC01 is developed for the multiple-capacitance measurement. One of the main applications of the MUXC01 concerns the accurate measurement of the multiple capacitances in combination with a capacitance-controlled oscillator. As an example, Figure 10 shows a diagram for such an application. In this application, a microcontroller is employed to provide control signals for the multiplexer and measure the output signal from the UTI. The UTI is a universal transducer interface for various passive sensors, for instance, the capacitive, resistive, resistive-bridge and potentiometric sensors. When the UTI is set in the mode CMUX, it works as a capacitance-controlled oscillator. The multiplexer(s) is used to select the capacitor(s) to be measured and provide driving signals with a square-wave form for the capacitances to be measured. By using the serial input and the clock input on the multiplexer, any of these capacitances in any combination can be measured.

B. Nine bit shift register

When the input signal of the MUXC01 is high (V_{CC}), the function of the multiplexer just is a 9 bit shift register with one data entry (*serial in*) and the output from each of the nine stages. So the multiplexer can be used as a 9 bit shift register.

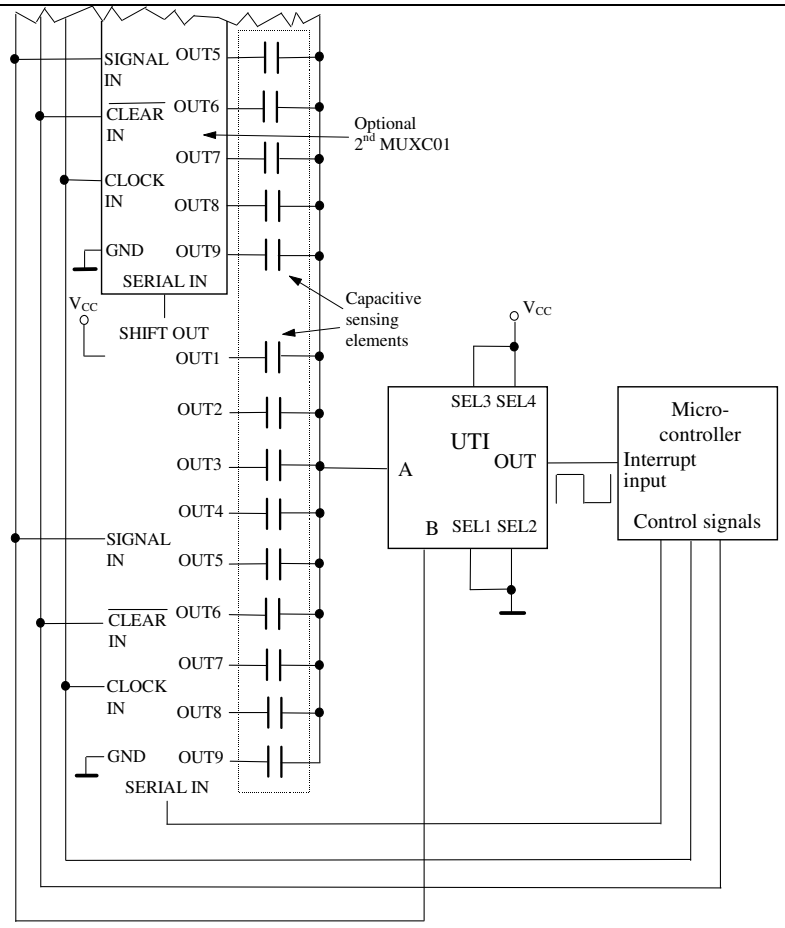


Figure 10 A diagram for the application of the MUXC01 in a multiple-capacitance measurement.

11. Chip Size

Figure 11 shows the pad configuration of the MUXC01. The size of the die amounts to 1.7 mm ×1.6 mm.

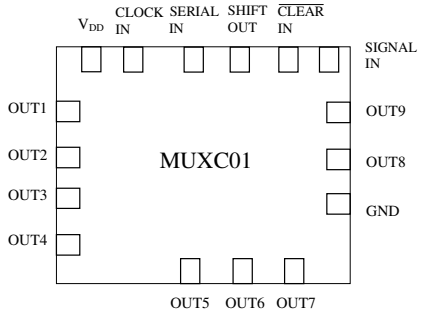


Figure 11 The pad configuration of MUXC01 chip.